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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,057	04/20/2001	Rajasekhar Cherabuddi	P4952	2317

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/839,057	CHERABUDDI ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because of unclear handwriting in the Figures. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 11-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Konigsburg; Brian R. et al. (US 6412051 B1, hereafter referred to as Konigsburg).

35 U.S.C. 102(e) rejection of claim 11.

Konigsburg teaches a multiple-way associative cache memory (see Abstract, Konigsburg; Note: an n-way set associative cache is a multiple-way associative cache memory), comprising: a plurality of cache blocks, each having a number of cache lines to store data (see n-way set associative cache 50 in Figure 2 of Konigsburg); a plurality of tag arrays, each storing a number of tags for associated data in a corresponding one of the plurality of cache blocks (Tag array 30 in Figure 2 of Konigsburg comprises a plurality of tag arrays, one for each way of the n-way set associative cache 50, each storing a number of tags for associated data in a corresponding one of the plurality of cache blocks); and select means connected to both the cache blocks and the tag arrays (comparator 28, Encoder 44 and multiplexor 52 in Figure 2 of Konigsburg is a select means connected to both the cache blocks and the tag arrays), the select means configured to selectively disable one or more of the plurality of cache blocks (col. 2, lines 57-62, Konigsburg teaches that the Invalid flag of MESI field 38 is used to inhibit, i.e., selectively disable, access to a cache set, i.e., way, for which one or more failures have been determined).

35 U.S.C. 102(e) rejection of claim 12.

Konigsburg teaches a plurality of memory devices, each for storing a way select value for a corresponding cache block (see Tag Array 30 and Tag field 34 in Figure 2 of Konigsburg; Note: col. 2, lines 57-62, Konigsburg teaches that the Invalid flag of MESI field 38 is used to inhibit, i.e., selectively disable, access to a cache set, i.e., way, for which one or more failures have been determined; hence Tag Address 22 is a Way

Select Value since it is used to select a corresponding MESI field 38 in the tag array 30); a plurality of gating circuits (Comparator 28 in Figure 2 of Konigsburg comprises a plurality of gating circuits), each having a first input terminal coupled to receive a match signal from a corresponding tag array (Tag Fields 34 in Figure 2 of Konigsburg are match signals from a corresponding tag array), a second input terminal coupled to receive a corresponding way select value (Tag Address 22 in Figure 2 of Konigsburg is a Way Select Value since it is used to select a corresponding MESI field 38 in the tag array 30), and having an output terminal to provide a gated match signal for a corresponding cache block (Note: a gated match signal is provided to Encoder 44 in Figure 2 of Konigsburg).

35 U.S.C. 102(e) rejection of claims 13 and 14.

Konigsburg teaches an encoder circuit having a plurality of input terminals coupled to receive the gated match signals for corresponding cache blocks, and having an output terminal to provide a select signal (Encoder 44 in Figure 2 of Konigsburg is an encoder circuit having a plurality of input terminals coupled to receive the gated match signals for corresponding cache blocks from Comparator 28, and having an output terminal to provide a select signal); and a multiplexer having a plurality of input terminals coupled to receive data from corresponding cache blocks, an output terminal to provide output data, and a control terminal to receive the select signal (Multiplexer 52 is a a multiplexer having a plurality of input terminals coupled to receive data from corresponding cache

blocks in Cache 50, an output terminal 54 to provide output data, and a control terminal to receive the select signal from Encoder 44).

35 U.S.C. 102(e) rejection of claim 15.

Konigsburg teaches that the way select signals selectively disable corresponding cache blocks by forcing corresponding match signals to a mismatch condition (Note: Figure 2 in Konigsburg teaches a tag array 30 in Figure 2 of Konigsburg having a one-to-one correspondence between sets and lines in an N-way associative cache memory; col.2 lines 35-62 in Konigsburg teaches forcing a comparison between a requested tag address 22 and tags in tag array 30 corresponding to cache lines in the disabled cache block to a mismatch condition so that the disabled cache block is not selected for the cache read operation; Note also if the flag inhibitor of MESI field 38 is set to inhibit, a mismatch condition will be forced to inhibit the selection of the way).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asher; David H. et al. (US 6671822 B1, hereafter referred to as Asher) in view of DeKarske; Clarence W. (US 4168541 A).

35 U.S.C. 103(a) rejection of claims 1, 3 and 7.

Asher teaches a method of improving yield in a multiple way associative cache memory having a plurality of cache blocks each corresponding to one of the multiple ways, the method (col. 2, lines 60-65 in Asher teaches that current state of the art prior art Figure 1 provides for segmenting set associative cache into sets or ways whereby a set or way can be disabled, if a defect is found in the memory area or block associated with the set or way during manufacturing to increase yield, since the defective set associative cache can still be used with degraded memory capacity) comprising: for each way, selectively disabling the way, if the corresponding cache block is defective (col. 2, lines 60-65 in Asher teaches that current state of the art prior art Figure 1 provides for segmenting set associative cache into sets or ways whereby a set or way can be selectively disabled during manufacture, if a defect is found in the memory area or block associated with the set or way). Note: Asher teaches operating the remaining, non-disabled cache blocks as a less-associative or n-1-way associative cache memory (col. 2, lines 60-65 in Asher

teaches that the cache can still be used as a smaller usable cache, i.e., a less-associative or n-1-way associative cache memory, with the way disabled).

However Asher does not explicitly teach the specific step of determining whether a defect exists in any of the cache blocks.

DeKarske, in an analogous art, teaches Error Checking Circuits for detecting whether a defect exists in any of the cache blocks corresponding to a way of an N-way set associative cache memory (col. 6, lines 67-68 & col.7, lines 1-4). Note: the Prior Art method taught in Asher requires knowledge of defective blocks within a way in order to function, i.e., in order to implement the method in the Asher patent, and DeKarske teaches a step and a means for detecting defective blocks within a way, hence one of ordinary skill in the art at the time the invention was made would have been highly motivated to combine the teachings in the Asher and DeKarske patents in order to implement the method taught in the Asher patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Asher with the teachings of DeKarske by including an additional step of determining whether a defect exists in any of the cache blocks. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that determining whether a defect exists in any of the cache blocks would have provided the opportunity to implement the method taught in the Asher patent.

4. Claims 2, 4-6 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asher; David H. et al. (US 6671822 B1, hereafter referred to as Asher) and DeKarske; Clarence W. (US 4168541 A) in view of Konigsburg; Brian R. et al. (US 6412051 B1, hereafter referred to as Konigsburg).

35 U.S.C. 103(a) rejection of claims 2 and 8.

Asher and DeKarske substantially teaches the claimed invention described in claim 1 (as rejected above).

However Asher and DeKarske do not explicitly teach the specific use of storing a way select value indicative of whether the corresponding cache block is defective.

Konigsburg, in an analogous art, teaches a MESI field 38 in Figure 2 of Konigsburg for storing flags for indicating that a particular line has either been Modified, is Exclusive, is Shared, or is Invalid whereby the Invalid flag of MESI field 38 is used to inhibit access to a cache set, i.e., way, for which one or more failures have been determined (col. 2, lines 57-62, Konigsburg). Note: the Prior Art method taught in Asher teaches a set or way can be disabled, if a defect is found in the memory area or block associated with the set or way during manufacturing to increase yield (col. 2, lines 60-65 in Asher), but does not teach the specific mechanisms required to implement such a method. Konigsburg, on the other hand teaches the necessary mechanisms for implementing the Prior Art method taught in the Asher patent, hence one of ordinary skill in the art at the time the invention was made would have been highly motivated to combine the teachings in the

Asher and DeKarske patents with the teachings in the Konigsburg patent in order to implement the method taught in the Asher and DeKarske patents.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Asher and DeKarske with the teachings of Konigsburg by including an additional step of storing a way select value indicative of whether the corresponding cache block is defective. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that storing a way select value indicative of whether the corresponding cache block is defective would have provided the opportunity to implement the method taught in the Asher and DeKarske patents.

35 U.S.C. 103(a) rejection of claims 4 and 9.

Konigsburg teaches forcing a comparison between a requested tag address and tags corresponding to cache lines in the disabled cache block to a mismatch condition so that the disabled cache block is not selected for the cache read operation (Note: Figure 2 in Konigsburg teaches a tag array 30 in Figure 2 of Konigsburg having a one-to-one correspondence between sets and lines in an N-way associative cache memory; col.2 lines 35-62 in Konigsburg teaches forcing a comparison between a requested tag address 22 and tags in tag array 30 corresponding to cache lines in the disabled cache block to a mismatch condition so that the disabled cache block is not selected for the cache read operation; Note also if the flag inhibitor of MESI field 38 is set to inhibit, a mismatch condition will be forced to inhibit the selection of the way).

35 U.S.C. 103(a) rejection of claims 5 and 10.

Konigsburg teaches comparing the requested tag address with tags corresponding to the disabled cache block (col. 2, lines 41-45 in Konigsburg teach comparing the requested tag address 22 with tags corresponding to the disabled cache block in tag array 30); generating, for each cache block, a match signal indicating the results of the comparing step (col. 2, lines 41-45 in Konigsburg teach generating, for each cache block, a match signal indicating the results of the comparing step); and gating the match signals with corresponding way select values to selectively force the mismatch condition for comparison results corresponding to the disabled cache block (Note; if the flag inhibitor of MESI field 38 is set to inhibit, a mismatch condition will be forced to inhibit the selection of the way).

35 U.S.C. 103(a) rejection of claim 6.

Col. 2, lines 60-65 in Asher teaches that current state of the art prior art Figure 1 provides for segmenting set associative cache into sets or ways whereby a set or way can be selectively disabled during manufacture, if a defect is found in the memory area or block associated with the set or way.

5. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Konigsburg; Brian R. et al. (US 6412051 B1, hereafter referred to as Konigsburg).

35 U.S.C. 103(a) rejection of claims 16.

Konigsburg substantially teaches the claimed invention described in claims 11-15 (as rejected above).

However Konigsburg does not explicitly teach the specific use of fuses.

The Examiner asserts that it would be an obvious engineering design choice to select a memory comprising fuses since Konigsburg teaches an arrayed memory for storing tag information but does not explicitly teach the make-up of the tag memory array. One of ordinary skill in the art at the time the invention was made would have been motivated to use fuses since fuses are read only memory and only need to be set once.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Konigsburg by including use of fuses.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of fuses would have provided the opportunity to implement a read only permanent memory portion of the Tag memory array for storing information on permanent defects.

35 U.S.C. 103(a) rejection of claim 17.

Konigsburg substantially teaches the claimed invention described in claims 1-15 (as rejected above).

However Konigsburg did not explicitly teach the specific use of AND gates.

The Examiner asserts that AND gates are commonly used circuits for disabling an output and Konigsburg teaches a circuit whereby a way is disabled in response to an inhibit signal, hence one of ordinary skill in the art at the time the invention was made would have been motivated to use AND gates to inhibit or disable a signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Konigsburg by including an additional step of use of AND gates. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of AND gates would have provided the opportunity to inhibit or disable a signal.

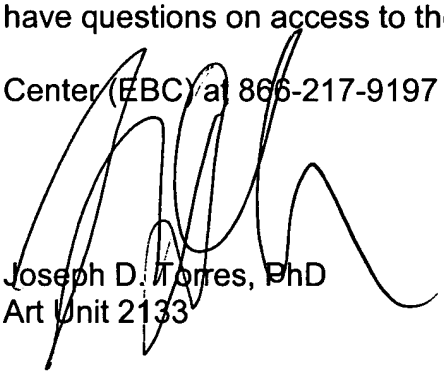
Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Pereira; Jose Pio (US 6687785 B1) teaches semiconductor memories and specifically to content addressable memories. McClure; David Charles (US 5666482 A) teaches set associative cache memories. Keeley; James W. et al. (US 4464717 A) teaches cache systems includable within minicomputer and microprocessing systems. Green; Daniel W. (US 5940858 A) teaches microprocessors that implement cache circuits with programmable sizing. Array Word Redundancy Scheme, IBM Technical Disclosure Bulletin, August 1982, volume 55, Issue 3A, pages 989-992.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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